REMARKS

The Examiner is thanked for the thorough consideration given the present application.

Claims 1-17 are pending in the present application. Claims 7, 10 and 17 have been amended.

Reconsideration of the application, as amended, is respectfully requested.

Claim for Priority

It is gratefully acknowledged that the Examiner has recognized the Applicant's claim for foreign priority. In view of the fact that the Applicant's claim for foreign priority has been perfected, no additional action is required from the Applicant at this time.

Drawings

It is gratefully acknowledged that the Official Draftsperson has approved the Formal Drawings submitted by the Applicants. The drawings comply with the requirements of the USPTO. No further action is necessary.

Allowable Subject Matter

Applicant greatly appreciates the Examiner's indication in the outstanding Office Action that claims 10 and 17 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As will be seen by the above amendments, claim 10 has been rewritten in independent form including all of the limitations of base claim 1. In addition, claim 17 has been rewritten in independent form including all of the limitations of base claim 11.

Accordingly, it is believed that claims 10 and 17 are now in condition for immediate allowance.

Claim Rejection – 35 U.S.C. § 112

Claim 7 stands rejected under 35 U.S.C. § 112, second paragraph, as lacking antecedent basis for certain limitations in the claim. This rejection is respectfully traversed.

Claim 7 has been amended to depend from claim 2, as kindly suggested by the Examiner. Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 112 are respectfully requested.

Claim Rejections – 35 U.S.C. § 103

Claims 1, 4-5, and 8-9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Asada et al. (U.S. Patent 5,883,609 – hereinafter "Asada") in view of Wood et al. (U.S. Patent 5,926,162 – hereinafter "Wood"). Claims 2-3, 7, and 11-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Asada in view of Wood, and in further view of Kurz (U.S. Patent 4,810,973). Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Asada in view of Wood, and in further view of Yamaguchi et al. (U.S. Patent 5,307,084 – hereinafter "Yamaguchi"). Claims 15 and 16 stand rejected under 35 U.S.C. § 103(a) as being

unpatentable over Asada in view of Kurz, and in further view of Yamaguchi. These rejections are respectfully traversed.

The Section 103 rejections over Asada, Wood, Kurz and Yamaguchi are believed to be improper because one of ordinary skill in the art would not be motivated by the cited art, either alone or in combination, to modify the corrected voltage generating means of present claim 1 or the first detection terminal of present claim 11 for the reasons set forth below.

In order for a claim to be properly rejected under 35 U.S.C. § 103, the teachings of the prior art reference must suggest all features of the claimed invention to one of ordinary skill in the art. *See, e.g., In re Dow Chemical*, 837 F.2d 469, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988); *In re Keller*, 642 F.2d 413, 208 U.S.P.Q. 871, 881 (C.C.P.A. 1981). The teachings of Asada, Wood, Kurz, and Yamaguchi do not disclose or suggest all of the features of the claimed invention. Thus, the rejection of independent claim 1 under 35 U.S.C. § 103(a) should be withdrawn.

Independent, the claim 1 recites.

> 1. " An image display device comprising a plurality of gate buses, a plurality of source buses, transistors each of which for supplying a pixel electrode with a voltage from said source bus, a common electrode, and a corrected voltage supplying means for supplying said common electrode with a common electrode voltage which has been corrected by an amount of correction,
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> wherein said corrected voltage supplying means comprising:
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> a changing voltage generating means for generating a first changing voltage having changing voltage levels for setting said transistor to an on-state and a second changing voltage having changing voltage levels for setting said transistor to an off-state, said changing voltage generating means operating so as to establish at least three supply modes including a first supply mode, a second supply mode and a third supply mode, said first supply mode in which

said first changing voltage is supplied to a first number of ones of said plurality of gate buses and said second changing voltage is supplied to a second number of ones of said plurality of gate buses, said second supply mode in which said first changing voltage is supplied to a third number of ones of said plurality of gate buses and said second changing voltage is supplied to a fourth number of ones of said plurality of gate buses or said first changing voltage is supplied to at least said third number of ones of said plurality of gate buses and said second changing voltage is not supplied to said plurality of gate buses, and said third supply mode in which said first changing voltage is supplied to a fifth number of ones of said plurality of gate buses and said second changing voltage is supplied to a sixth number of ones of said plurality of gate buses or said first changing voltage is not supplied to said plurality of gate buses and said second changing voltage is supplied to at least said sixth number of ones of said plurality of gate buses; and

a corrected voltage generating means for detecting, each time each of said at least three modes is established, a voltage on said common electrode to determine said amount of correction on the basis of amounts of change in said detected voltages on said common electrode. " (Emphasis added.)

Comparing the present invention with Asada and Wood, Asada and Wood do not suggest the corrected voltage generating means for supplying said common electrode with a common electrode voltage which has been corrected by an amount of correction and a corrected voltage generating means for detecting a voltage on said common electrode to determine said amount of correction on the basis of amounts of change in said detected voltages on said common electrode, as set forth in present claim 1.

Col. 9, lines 23-32 of Wood states that,

"The summed signal from the combiner summing circuit 510 and the display average signal from the display signal averaging circuit 400 are provided to the amplifier 512, which generates an appropriate common electrode 114 voltage in accordance with the combiner summed signal and the display average signal. In the present embodiment, the amplifier 512 comprises a conventional operational amplifier having a noninverting input and an

inverting input. The display average signal is provided to the noninverting input and the combiner summed signal is provided to the inverting input."

Referring to FIG. 5 of Wood, the amplifier 512 obtains the common voltage according to $V_{SOURCE+}$, $V_{SOURCE-}$, V_{TEMP}, and V_{GATE}. However, $V_{SOURCE+}$, $V_{SOURCE-}$, V_{TEMP}, and V_{GATE} are not voltage of the common electrode.

Col. 6, lines 30-48 of Wood states:

"In accordance with a preferred aspect of the present invention, a main point in the acquisition of the null component of the common plane voltage which is the output of 504 is to obtain the average, **the output of 502 of the minimum and maximum voltage drive to the source lines (V source - and V source +)** the input to 502 of the LCD. The method for determining the V source - and V source + drive voltages to the source lines is dependent on the method the source driver chip uses to either apply or generate the source voltages. Some types of drivers apply the minimum and maximum reference voltages from external supply circuitry, while other types of drivers generate the minimum and maximum reference voltages internally. Preferably, the method of determining the null component of the common plane voltage involves utilizing a spare output or outputs of a source driver or drivers and sampling them at a controlled input value to generate the V source - and V source + reference voltages at the output, then averaging them for the null component of the common plane voltage." (Emphasis added.)

As discussed above, $V_{SOURCE+}$ and $V_{SOURCE-}$ respectively indicate the maximum voltage and the minimum voltage of the source lines.

Col. 8, lines 53-65 of Wood states:

"The signal received from the temperature sensor 408 is processed by the temperature compensation signal generator 404 to provide a signal corresponding to the temperature of the liquid crystal layer 106 and which may be used to control the voltage applied to the common electrode 114 accordingly. For example, **the temperature signal generator 404 suitably includes a temperature divider circuit 508, such as a voltage divider circuit, which divides the signal received from the temperature sensor 408 by a temperature constant.** The temperature constant suitably comprises a

preselected constant based on the type of liquid crystal and the configuration of the LCD 100, and is typically in the range of 150 mV from -40°C. to +85°C." (Emphasis added.)

As discussed above, V_{TEMP} indicates temperature.

As set forth in Col. 7, line 61 through Col. 8, line 19, of Wood:

> "**The rectified signal is provided to a parasitic capacitance compensation circuit 506, which divides the rectified signal by a suitable gate parasitic constant.** The gate parasitic constant is determined based on the LCD 100 configuration, suitably at the factory when the LCD 100 is assembled, and is typically in the range of approximately 10. Gate parasitic capacitance is primarily affected by the misalignments which occur during manufacture of the TFT. For example, the gate parasitic constant may be a function of the thickness of the gate insulator and the TFT 208 alignment, both of which are set during the fabrication process of the LCD 100. Gate parasitic capacitance is primarily affected by the misalignments which occur during manufacture of other TFT. Primary factors in the parasitic gate constant are: variation in C_{as} due to manufacturing tolerance variation in $C_{storage}$ due to manufacturer tolerance variation in gate drive voltage (peak-to-peak) rate of change in gate drive voltage ($C^{dV}/_{dC}$). Consequently, the gate parasitic constant is suitably adjustable so that the appropriate value for the constant may be determined when the LCD 100 is assembled and then set accordingly. Alternatively, any other suitable mechanism may be provided to determine the appropriate gate parasitic constant and generate the appropriate parasitic capacitance compensation signal. Thus, any LCD 100 may be individually adjusted to operate using the appropriate gate parasitic constant." (Emphasis added.)

Accordingly, V_{GATE} indicates a suitable gate parasitic constant. In Wood, the amplifier 512 does not utilize the voltage of the common electrode to determine an amount of correction. Thus, Wood fails to disclose that the corrected voltage generating means for supplying said common electrode with a common electrode voltage which has been corrected by an amount of correction and a corrected voltage generating means for detecting a voltage on said common

electrode to determine said amount of correction on the basis of amounts of change in said detected voltages on said common electrode, as set forth in present claim 1.

Since neither Asada nor Wood disclose, suggest or teach all the features recited by claim 1 of the present application, Asada and Wood cannot render claim 1 anticipated or obvious, and claim 1 should be allowable over the references of record.

For the same reasons set forth above in connection with claim 1, neither Kurz nor Yamaguchi cure the deficiencies of Asada and Wood. Consequently, there would be no motivation for one skilled in the art to modify Asada, Wood, Kurz, and Yamaguchi, either alone or in combination, to reach the corrected voltage generating means of present claim 1. Accordingly, the rejection of the claim 1 under 35 U.S.C § 103(a) is believed to be improper. Therefore, claim 1 is believed to be allowable for the reasons set forth above.

Dependent claims 2-9 are also believed to be allowable for at least the reason that these claims depend from allowable independent claim 1. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 103 are respectfully requested.

With regard to the rejections of claims 11-14, 15 and 16, as set forth in the outstanding Office Action, in order for a claim to be properly rejected under 35 U.S.C. § 103, the teachings of the prior art reference must suggest all features of the claimed invention to one of ordinary skill in the art. *See, e.g., In re Dow Chemical*, 837 F.2d 469, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988); *In re Keller*, 642 F.2d 413, 208 U.S.P.Q. 871, 881 (C.C.P.A. 1981). The teachings of

Asada, *Wood*, *Kurz*, and *Yamaguchi* do not suggest all of the features of the claimed invention to one of ordinary skill in the art. Thus, the rejection of claim 11 under 35 U.S.C. § 103(a) should be withdrawn.

Independent, claim 11 is as follows.

> 11. "An image display device comprising a plurality of gate buses, a plurality of source buses, transistors each of which for supplying a pixel electrode with a voltage from said source bus, a common electrode, and a corrected voltage supplying means for supplying said common electrode with a common electrode voltage which has been corrected by an amount of correction,
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> wherein said corrected voltage supplying means comprising:
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> a changing voltage generating means for generating a first changing voltage having changing voltage levels for setting said transistor to an on-state and a second changing voltage having changing voltage levels for setting said transistor to an off-state, said changing voltage generating means operating so as to establish at least three supply modes including a first supply mode, a second supply mode and a third supply mode, said first supply mode in which said first changing voltage is supplied to a first number of ones of said plurality of gate buses and said second changing voltage is supplied to a second number of ones of said plurality of gate buses, said second supply mode in which said first changing voltage is supplied to a third number of ones of said plurality of gate buses and said second changing voltage is supplied to a fourth number of ones of said plurality of gate buses or said first changing voltage is supplied to at least said third number of ones of said plurality of gate buses and said second changing voltage is not supplied to said plurality of gate buses, and said third supply mode in which said first changing voltage is supplied to a fifth number of ones of said plurality of gate buses and said second changing voltage is supplied to a sixth number of ones of said plurality of gate buses or said first changing voltage is not supplied to said plurality of gate buses and said second changing voltage is supplied to at least said sixth number of ones of said plurality of gate buses;
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> **a first detection terminal for detecting a voltage on said common electrode each time each of said at least three modes is established;**
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> a storing means for storing said corrected common electrode voltage which is determined on the basis of amounts of change in said detected voltages on said common electrode through said first detection terminal; and

> a DA converting means supplied with said corrected common electrode voltage stored in said storing means as a digital signal, said DA converting means converting said supplied digital signal into an analog voltage and outputting said analog voltage to said common electrode." (Emphasis added.)

Comparing the present invention with Asada and Kurz, Asada and Kurz do not specifically teach a first detection terminal for detecting a voltage on said common electrode. Since Kurz does not disclose that the AD is capable of detecting the voltage on the common electrode, one of ordinary skill in the art would have no motivation to utilize Kurz to reach the first detection terminal for detecting a voltage on said common electrode.

Yamaguchi fails to cure the deficiencies of Kurz. Consequently, there would be no motivation or suggestion to one skilled in the art to utilize Asada, Wood, Kurz, and Yamaguchi to achieve a first detection terminal for detecting a voltage on said common electrode, as set forth in claim 11. Accordingly, the rejection of the claim 11 under 35 U.S.C § 103(a) is believed to be improper. Dependent claims 12-16, which depend directly or indirectly on claim 11, are also believed to be allowable at least for the reasons set forth above and because these dependent claims contain all of the features/elements/steps of independent claim 11. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Accordingly, reconsideration and withdrawal of the rejections of the claims under 35 U.S.C. § 103 are respectfully requested.

Conclusion

In view of the above amendments and remarks, Applicant believes the pending application is in condition for allowance, and an early Notice of Allowance is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned, at the telephone number below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

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